Tutorial1

T1: Title of the Tutorial: Taking Reuse to Next Level: Exploiting Transaction Level Modeling (TLM) for Universal Verification Methodology (UVM).

Abstract of the tutorial

Verification engineers, EDA suppliers, service providers, and others throughout the electronics industry are actively creating verification environments following the UVM principles. Concepts like stimulus generation based on sequences, test execution using phases, communication based on Transaction-Level Modeling (TLM), all have significantly contributed to the maturity of functional verification practices involving UVM. The adoption of a common TLM standard across both SystemVerilog test benches and SystemC reference models makes good sense for everyone. The proposed Tutorial aims to provide- An introduction to "IEEE 1666-2011 SystemC standard", new SystemC modelling elements introduced in SystemC 2.3.1, an introduction to the role of TLM abstraction in UVM 1.2 including involved modelling techniques & guidelines and its usability for early Embedded Software Development, functional verification and SoC architecture exploration.

Biography of Speaker:

Nishit Gupta

He is working as Scientist in 'R&D in Electronics Group' at 'Ministry of Electronics & information Technology', Government of India. Earlier, he has worked as Technical Leader in 'Technology- R&D Group' at ST Microelectronics for around 9 years, wherein he was involved in developing and promoting across various ST sites the System Level Methodologies around TLM/ SystemC, Debug/ Verification tools & hardware IPs for SOC Architecture Analysis & Performance Evaluation at an early design phase.