Tutorial 2

T2: Title of the Tutorial: Recent Trends in Modeling and Simulation of Defects in Analog Circuits and their Applications

Abstract

While there has been tremendous improvement in detecting and testing defects, modeled as faults, in digital circuits over the last 20 years, there is no industry standard analog fault model till date for AMS circuits. In this tutorial, we will look at new methods for modeling and simulating different types of faults in AMS circuits using a novel mixed- signal fault injection methodology. The main contributions are two-fold: (i) Modeling defects in analog circuits using different fault models, along with techniques to reduce redundancy in faults and (ii) Use of transient analyses that leverage different methods to inject faults in the analog circuit and run simulation, thereby calculating fault coverage based on deviations from the fault-free circuit simulation results. These were tried and tested on two industrial cases using the commercially available Cadence® Spectre® simulator. It is expected that such analog fault simulation flows will be increasingly required as more mixed-signal designs find their applications in various industry segments.

Biography of Speaker:

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Vijay Kumar Sankaran is a Principal Applications Engineer at Cadence Design Systems (India) Pvt. Ltd., Bangalore with more than 10 years of experience in the field of Analog and Mixed Signal SoC Verification and Application support. Vijay is primarily responsible for supporting IC designers and verification engineers by driving AMS design & verification methodologies, including low power mixed-signal verification, mixed-signal functional safety analysis and mixed-signal fault simulations. Vijay holds B.E in Electronics and Communication Engineering from Anna University, Chennai and M.Tech. in Microelectronics from Birla Institute of Technology and Science, Pilani.