

Tutorial 3

T3: Title of the Tutorial: Tunnel Field Effect Transistors and Re-configurable Device: A New Paradigm in Emerging Device Technology

Abstract: The down scaling of MOS technology suffers from various Short Channel Effects (SCE) and motivated the researchers to propose some innovative/emerging devices to offset the SCEs. The idea to incorporate the Zener Tunneling Phenomenon in the Field Effect Transistors is an imaginative area with which we can remove the fundamental limits of MOS technology like power dissipation, steep sub-threshold slope, small OFF current and the reduction of the supply voltage. The domain of Tunnel FETs proclaims that we can achieve the better performance in terms of Sub-threshold Slope, OFF current, quantum tunneling phenomenon in which the carrier tunnels through the potential barrier and hence it does not have any limitation on Sub-threshold slope like conventional MOSFETs. We have also presented a concise discussion on Reconfigurable Nanowire FETs which is having the capability to provide n-type and p-type behavior in a single transistor. This is basically a Schottky Junction device with doping-less channel. The advantages of these technological nodes are attractive in circuit applications, where the chip requires fewer transistors to achieve a better performance.

Biography of Speaker:



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S. Dasgupta, is presently working as an Associate Professor, in Microelectronics and VLSI Group of the Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee. He received his PhD degree in Electronics Engineering from Institute of Technology-Banaras Hindu University (currently IIT-BHU), Varanasi in 2000. He has authored/co-authored more than 200 research papers in peer reviewed international journals and conferences. His citations are around 2400 (after 2006) and h-index and i-index are 25 and 65 respectively. He is a member of IEEE, EDS, ISTE and associate member of Institute of Nanotechnology, UK. He is also in the project evaluation committee of DST (Device Modelling and Simulation Group) and MEITY, GoI (Device-Circuit Co-Design Group). He has been a technical committee member International Conference on Micro-to-Nano, 2006; VDAT-2012, 13, 14, 15, 16, 17 and 18. He worked as the Organising Chair and Program Co-Chair for VDAT-2017 held at IIT Roorkee.