22nd International Symposium on VLSI Design and Test (VDAT2018)

28th June- 30th June2018

Thiagarajar College of Engineering, Madurai, Tamilnadu, India

VLSI Society of India
www.vlsi-india.net/vsi

Day 1 (28.06.2018)	**Time**	**Topic**	
	8:30 am – 9:30 am	Registration	
	9:30 am – 12:30 pm	Tutorial Track - T1 Venue: Mechanical Seminar Hall	Tutorial Track - T2 Venue: CSE Seminar Hall
		Topic : Taking Reuse to Next Level: Exploiting Transaction Level Modeling (TLM) for Universal Verification Methodology (UVM) ***Speaker 1 :*** ***Mr. Nishit Gupta,*** Scientist, Microelectronics Development Division, Ministry of Electronics & Information Technology, Government of India, New Delhi. ***Speaker 2 :*** ***Mr.*** **Deepak Jharodia** Technical Leader, ST Microelectronics, New Delhi, India.	***Topic :*** Recent trends in Modeling and simulation of defects in analog circuits and their applications. ***Speaker 1:*** ***Mr. Vijay Kumar Sankaran,*** Principal Application Engineer, Cadence Design systems (India) Pvt Ltd, Bangalore, KA, India. ***Speaker 2 :*** ***Mr.*** **Nadeem Husain Tehsildar,** Embedded Processing, Texas Instruments (India) Pvt. Ltd., Bangalore, India
	2:00PM-5:00PM	Tutorial Track – T3 Venue: Mechanical Seminar Hall	Tutorial Track – T4 Venue: CSE Seminar Hall
		Topic: Tunnel Field Effect Transistors and Reconfigurable Device: A New Paradigm in Emerging Device Technology ***Speaker:*** ***Dr. Sudeeb Dasgupta,*** Asso. Prof, IIT, Roorkee	***Topic :*** IoT Security: the darker side of the cloud ***Speaker:*** ***Mr. Preet Yadav,*** Analog and Mixed Signal Lead, NXP Semiconductors, Noida, India.

Day 2 FN (29.06.2018)	9:30 am – 10:00 am	Inaugural Function Venue: KS Auditorium	
	10:00 am – 10 .45am	Keynote Talk – I Topic: VLSI Design and Test **Speaker: Prof. Vishwani D. Agrawal, Auburn University,** USA Venue: KS Auditorium	
	10.45 am – 11: 15 am	Keynote Talk – II Topic: Hardware Security Speaker: **Prof. Michiko Inoue, NAIST, Japan** Venue: KS Auditorium	
	11:15 am – 11:30 am	Tea/Coffee Break	
	11:30 am – 12:45 pm	**Session – 1A** **Topic: Digital Design** **Session Chair: Dr. Neel Gala** Venue: Mechanical Seminar Hall 1A.1[12]:Efficient Hardware-Software Co-designs of AES Encryptor and RS-BCH Encoder. *Mohamed AsanBasiri M, and Sandeep K Shukla* 1A.2[50]:High Level Synthesis and Implementation of Cryptographic Algorithm in AHIR platform. *Abhimanniu Raveendran, SanjayDhok, and RajendraPatrikar* 1A.3[81]:A Hardware Accelerator for Convolutional Neural Network using Fast Fourier Transform *Kala S, Babita Jose, Debdeep Paul, Jimson Mathew* 1A.4[217]:Reconfigurable VLSI-Architecture of Multi-Radix Maximum-A-Posteriori Decoder for New Generation of Wireless Devices *Rahul Shrestha, and Ashutosh Sharma*	**Session – 1B** **Topic: Analog and Mixed Signal Design** **Session Chair: Dr. Sudeeb Dasgupta** Venue: CSE Seminar Hall 1B.1[3]:A PVT Insensitive Low-power Differential Ring Oscillator *NishthaWadhwa, PydiBahubalindruni, and Sujay Deb* 1B.2[25]:Optimal Transistor Sizing of Full-Adder Block to Reduce Standby Leakage Power *Prateek Gupta, Shubham Kumar, and Zia Abbas* 1B.3[18]:A 31ppm/0C Pure CMOS Bandgap Reference By Exploiting Beta-Multiplier *Nagulapalli R, and Naresh Reddy* 1B.4[179]:Supply and Temperature Independent Voltage Reference Circuit in Subthreshold Region *KokkulaVineysarathi, Akash Joshi, and RaghavendraDeshmukh*

Day 2 AN (29.06.2018)	12:45 pm – 1:45 pm	LUNCH	
	1:45 pm – 2:30 pm	Keynote Talk – III Topic: Embracing RISC-V for Next Generation Computing Speaker: **Dr. Neel Gala, RISE Lab., IIT Madras** Venue: KS Auditorium	
	2:30 pm – 4:00 pm	**Session – 2A** **Topic: Hardware Security** **Session Chair: Prof. Michiko Inoue, NAIST**, Japan Venue: Mechanical Seminar Hall 2A.1[32]: A Novel Approach to detect Hardware Malware using Hamming Weight Model and One Class Support Vector Machine *P Saravanan, and B M Mehtre* 2A.2[52]: Detecting Hardware Trojans by Reducing Rarity of Transitions in ICs *TapobrataDhar, Surajit Kumar Roy, and ChandanGiri* 2A.3[113]: Enhanced Logical Locking for an Secured Hardware IP against Key-guessing Attacks *SreeRanjani* 2A.4[200]: SARP: Self Aware Runtime Protection against Integrity Attacks of Hardware Trojans *KrishnenduGuha, DebasriSaha, and AmlanChakrabarti*	**Session – 2B** **Topic: Micro Bio-fluidics** **Session Chair: Mr. Preet Yadhav** Venue: CSE Seminar Hall 2B.1[92]: Effective Method for Temperature Compensation in Dual Band Metal MEMS Resonator *AmolMorankar ,RajendraPatrikar* 2B.2[192]:Deadlock detection in Digital Microfluidics Biochip droplet routing *Jyotiranjan Swain, and SumantaPyne* 2B.3[214]: Fabrication of Molybdenum MEMs Structures using Dry and Wet Etching *Sandeep Singh Chauhan, Niharika J, and S.K. Manhas* 2B.4[178]: Continuous Flow Microfluidic Channel Design for Blood Plasma Separation *JagritiSrivastava, andRajendraPatrikar*
	4:00 pm – 4:30 pm	Tea/ Coffee Break	
	4:30 pm – 6:00 pm	Poster Presentation (Oral) **Session Chair: 1. Prof. Virendra Singh, IIT Bombay Session Chair: 2. Dr.V.Venkatasubramani, TCE.** Venue: KS Auditorium	
	6.15 pm – 6.45 pm	Banquet Talk **Topic:** Let's Innovate India Speaker: **Mr. Preet Yadhav, NXP Semiconductors, Noida, India** **Venue:** KS Auditorium	
	6:45 pm – 7:45 pm	Cultural Program **Venue:** KS Auditorium	
	7:45 pm Onwards	Banquet Dinner	

<table>
<tr><td rowspan="5">Day 3 FN
(30.06.2018)</td><td>9:00 am – 9:45 am</td><td colspan="2">Keynote – IV
Topic: SoC Design Trends, Challenges and First Pass Success
Speaker: Dr.Nagi Naganathan, Broadcom, USA
Venue: CSE Seminar Hall</td></tr>
<tr><td>9:45 am – 10:30 am</td><td colspan="2">Keynote – V
Topic: Low power Design
Speaker: Prof. Rajveer Singh Shekhavat, Manipal University, Jaipur
Venue: CSE Seminar Hall</td></tr>
<tr><td>10:30 am – 11:00 am</td><td colspan="2">Tea/Coffee Break
Poster Display</td></tr>
<tr><td>11:00 am – 12:30 pm</td><td>Session – 3A
Topic: VLSI Testing
Session Chair: Prof. Vishwani D. Agrawal
Venue: CSE Seminar Hall

3A.1[15]: A Novel Countermeasure against Differential Scan Attack in AES Algorithm
JayeshPopat, and Usha Mehta
3A.2[228]:Optimization of Test Wrapper length for TSV based 3D SOCs using a heuristic approach
TanusreeKaibartta, and Debesh Das
3A.3[222]:A Methodology to Design Online Testable Reversible Circuits
MrinalGoswami, Govind Raj, AronNarzary, and BibhashSen
3A.4[185]:Robust SRAM Cell Development for Single-Event Multiple Effects
Naga RaghuramChinnapurapu, Manohar Reddy Daivamdinne, Kishore Kumar Puli, andGauravKaushal</td><td>Session – 3B
Topic: Analog Circuits and Devices
Session Chair: Mr. Nishit Gupta
Venue: Mechanical Seminar Hall

3B.1[44]: Temperature Insensitive Low-Power Ring Oscillator using only n-type Transistors
NishthaRai, NishthaWadhwa, BhawnaTiwari, Pydi Ganga Mamba Bahubalindruni, and VaibhavAgarwal
3B.2[71]: Low-Power Switched Operational Amplifier using a-InGaZnO TFTs
SuprateekShukla, Pydi Ganga Bahubalindrun, BhawnaTiwari, and Pedro Baquinha
3B.3[151]: Threshold Voltage Investigation of Recessed Dual-Gate MISHEMT:Simulation Study
Preeti Singh, VandanaKumari, ManojSaxena, and Mridula Gupta
3B.4[166]: LEADER: Leakage Currents Estimation Technique for Aging Degradation Aware 16nm CMOS Circuits
Zia Abbas, Andleeb Zahra, and Mauro Olivieri</td></tr>
<tr><td>12:30 pm – 1:15 pm</td><td colspan="2">LUNCH</td></tr>
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<tr>
<td rowspan="2">Day 3 AN
(30.06.2018)</td>
<td>1:15 pm –2:45 pm</td>
<td>Session – 4A
Topic: Network-on-Chip
Session Chair: 1. Dr.Nagi Naganathan
Venue: CSE Seminar Hall

4A.1[42]:Heuristic Driven Genetic Algorithm for Priority Assignment of Real-Time Communications in NoC
Ajay Khare, ChinmayPatil, ManikantaNallamalli , and SantanuChattopadhyaya

4A.2[55]:A Novel Fault-Tolerant Routing Algorithm for Mesh-of-Tree based Network-on-Chips
Monil Shah, MohitUpadhyay, Veda Bhanu P, Soumya J, and Linga Reddy Cenkeramaddi

4A.3 [97]:Performance Enhancement of NoCs using single cycle deflection routers and adaptive priority schemes
Midhula K S, SarathBabu, John Jose, Sangeetha Jose

4A.4[225] 3D LBDR : Logic Based Distributed Routing for 3D NoC
Ashsih Sharma, Manish Tailor, Lava Bhargava, and Manoj Gaur</td>
<td>Session – 4B
Topic: Memory
Session Chair: 1. Prof. Rajveer Singh Shekhavat
Venue: Mechanical Seminar Hall

4B.1[59]:Efficient and Failure aware ECC for STT-MRAM Cache Memory
Yogendra Gupta, KeerthiSagarKokkiligadda, and Lava Bhargava

4B.2[21]:A novel design approach to implement multi-port register files using pulsed latches
Manivannan T S, and MeenaSrinivasan

4B.3[73]:Low Leakage Noise Tolerant 10T SRAM Cell
Vinay Gupta, PratikshaShukla, and ManishaPattanaik

4B.4[98]:A Write-Improved Half-Select-Free Low-Power 11T Subthreshold SRAM with Double Adjacent Error Correction for FPGA-LUT Design
Vishal Sharma, PranshuBisht, AbhishekDalal, Shailesh Singh Chouhan, H. S. Jattana, SantoshVishvakarma</td>
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<tr>
<td>1:15 pm – 2:45 pm</td>
<td>PhD Forum
Session Chair 1: Dr.V.Vinoth Thyagarajan
TCE, Madurai
Session Chair 2: Dr.Gracia Nirmala Rani
TCE, Madurai
Venue: ECE Seminar Hall</td>
<td>Design Contest
Session Chair 1: Dr.S.Md. Mansoorroomi
TCE, Madurai
Session Chair 2: Dr.K.Hariharan
TCE, Madurai
Venue: Agilent Communication Lab</td>
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Day 3 AN (30.06.2018)	2:45 pm – 4:00 pm	**Session – 5A** **Topic: Quantum Computing and NoC** **Session Chair: Prof.Prathima Agrawal** Venue: CSE Seminar Hall 5A.1[89]: A Heuristic Qubit Placement Strategy for Nearest Neighbor Realization in 2D Architecture *AnirbanBhattacharjee, ChandanBandyopadhyay, LaxmidharBiswal, HafizurRahaman* 5A.2[191]:Quantum domain design of Clifford+T-based bidirectional Barrel Shifter *LaxmidharBiswal,AnirbanBhattacharjee,andHafizurRahaman* 5A.3[56]:Source Hotspot Management in a Mesh Network on Chip Shashank S Rao, SujayShaunak, SatyaSai Krishna Mohan G, Ajay S, Krutthika H K, Ananda Y R, and John Jose 5A.4 [7]:An Energy-Efficient Core Mapping Algorithm on Network on Chip (NoC) *B Naresh Reddy*	**Session – 5B** **Topic: Sensors and Interfaces** **Session Chair: Prof. Virendra Singh** Venue: Mechanical Seminar Hall 5B.1[37]: Fabrication and LBM-modeling of directional fluid transport on low-cost electrosomotic flow device *Pravinraj T, RajendraPatrikar* 5B.2[149]:Fully Digital, Low Energy Capacitive Sensor Interface with an Auto-Calibration Unit Chintanika, Chothani, and Biswajit Mishra 5B.3[197]:An Angular Steiner Tree Based Global Routing Algorithm For GrapheneNanoribbon Circuit *ArindamSinha Roy, Subrata Das, Pranab Roy, and HafizurRahaman*
	4.00 pm – 4.30 pm	**Tea/Coffee Break**	
	4:30 pm – 5:00 pm	**Valedictory Function**	